Partial Computation-skip Scheme for Power Supply Voltage Scaling

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WAPCO, HiPEAC @ Amsterdam 2015

OUTLINE

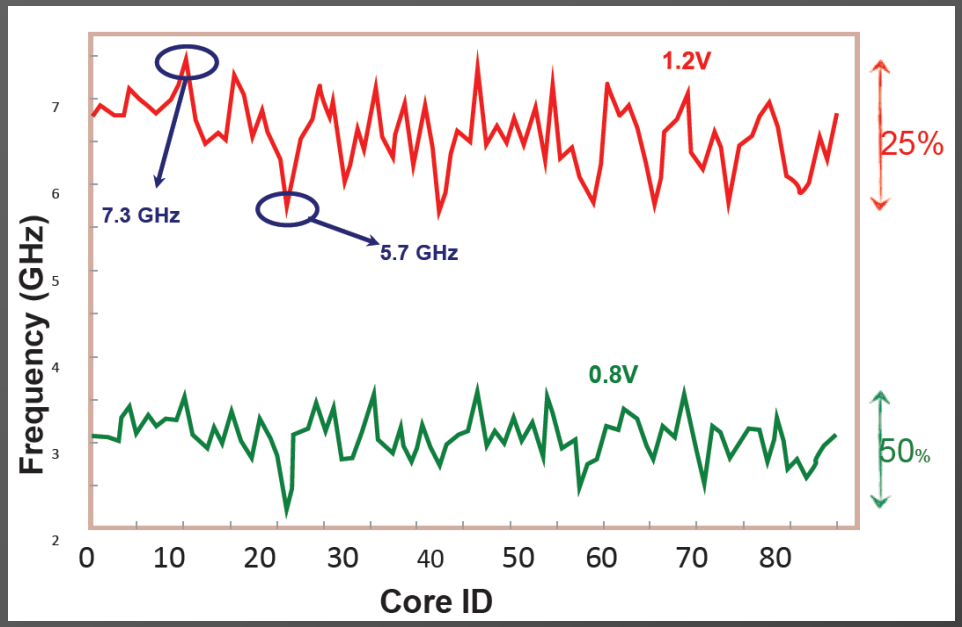
- Problem Statement

Partial CS (Computation-Skip) Scheme, CORDIC

Evaluation

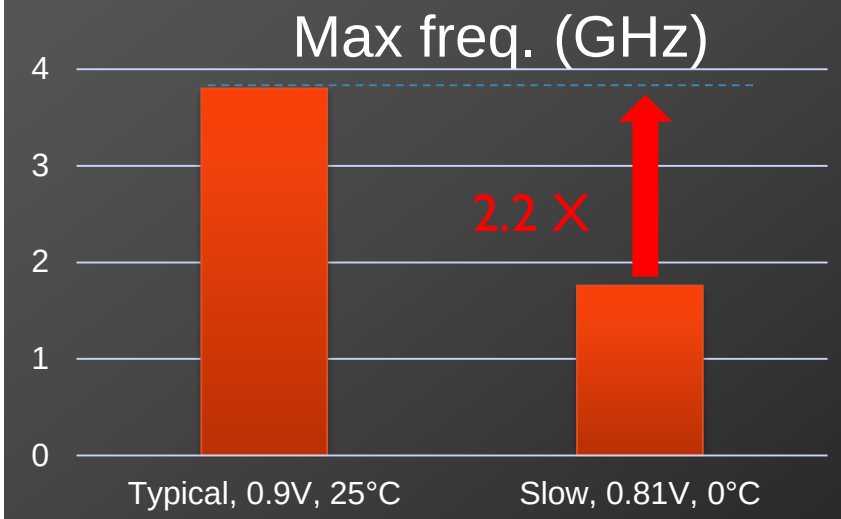
Conclusion

SEMICONDUCTOR VARIABILITY



65nm Intel

(2010 ISSCC, Dighe et el., "Within-die variation-aware dynamic-voltage-frequency scaling core mapping and thread hopping for an 80-core processor")



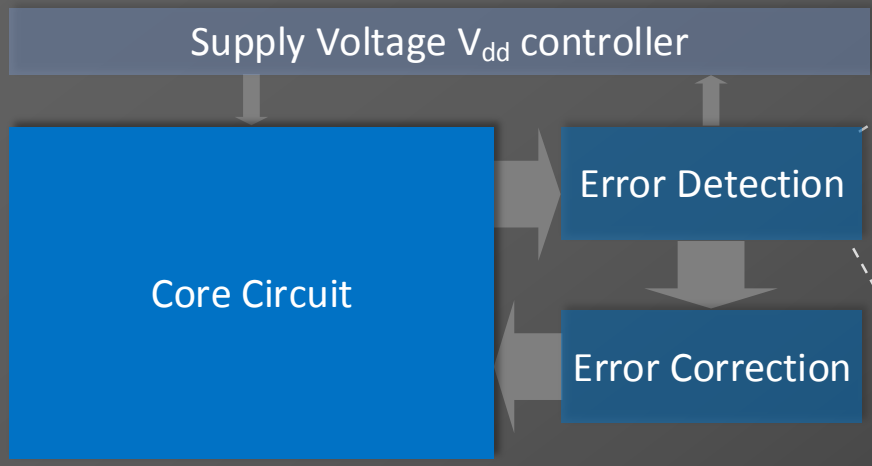
Today's technology imec, logic speed simulation under PVT variability

Process, Voltage, Temperature, Aging leads to variability

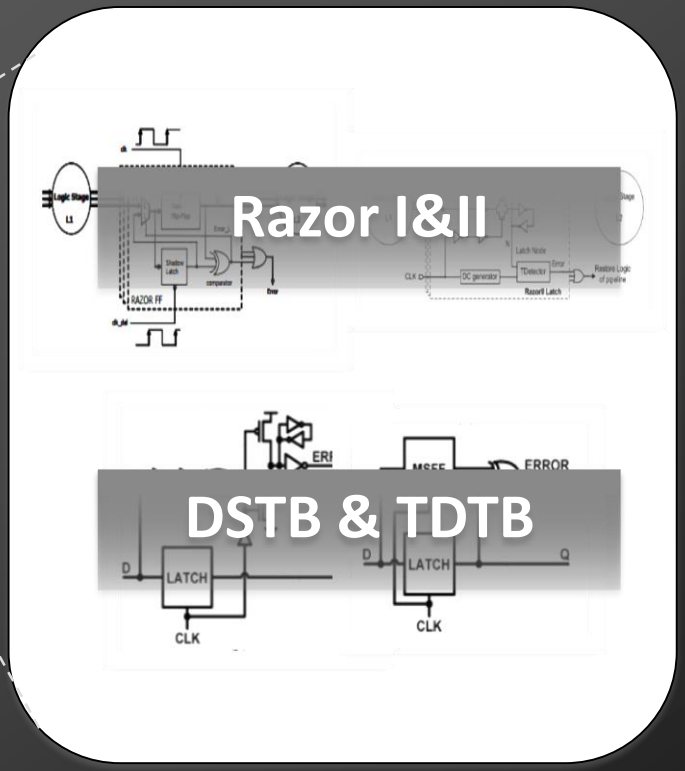
Variability demands huge timing margin

IC speed capability, power consumption, area are wasted

ON-CHIP VARIATION MONITORS



Check if data changes around clock edge



Setup timing violations are monitored

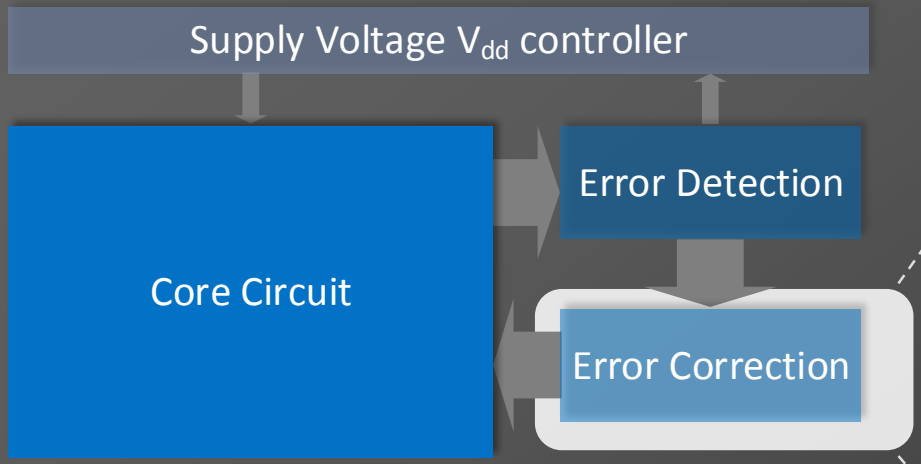
Operation parameters (V_{dd}, f_{clk}, T) changed accordingly to reduce further violations

Razor I: Ernst et al., 2003 MICRO, “Razor: a low-power pipeline based on circuit-level timing speculation”

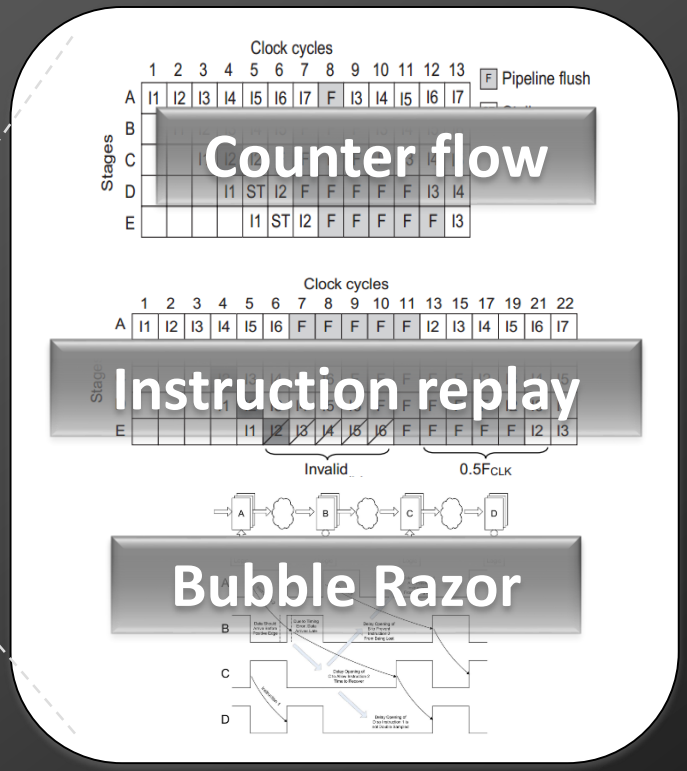
Razor II: Das et al., 2009 JSSC, "RazorII: In Situ Error Detection and Correction for PVT and SER Tolerance"

TDTB & DSTB: Bowman et al., 2009 JSSC, "Energy-efficient and metastability-immune resilient circuits for dynamic variation tolerance"

PRESENT ERROR CORRECT IS COSTLY



Stall and/or Flush the pipeline to compute with the correct data



☺ Error-free results for processors

☹ Multiple-cycle throughput penalty for each error (1% rule)

☹ Does NOT exploit the resilient from applications

Counter flow: Ernst et al., 2003 MICRO, “Razor: a low-power pipeline based on circuit-level timing speculation”

Instruction Replay: Das et al., 2009 JSSC, "RazorII: In Situ Error Detection and Correction for PVT and SER Tolerance"

Bubble Razor: Fojtik et al., 2013 JSSC, "Bubble Razor: Eliminating Timing Margins in an ARM Cortex-M3 Processor in 45 nm CMOS Using Architecturally Independent Error Detection and Correction"

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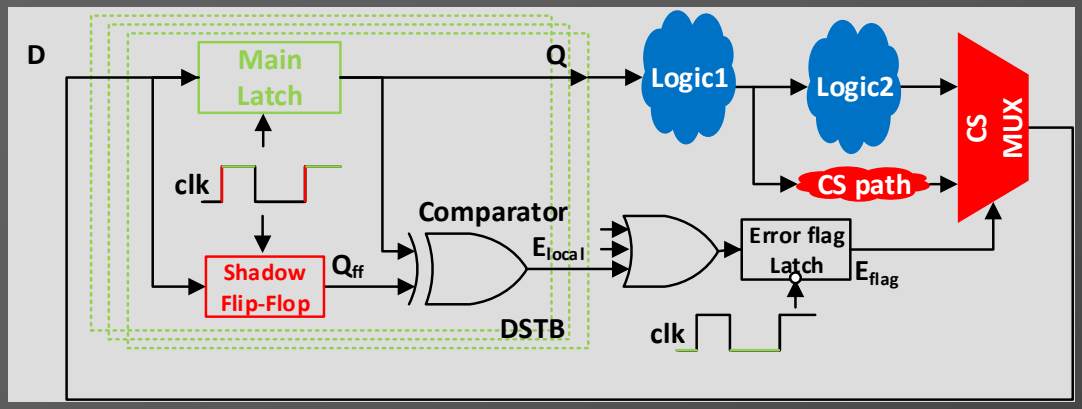
PARTIAL COMPUTATION-SKIP (CS) SCHEME

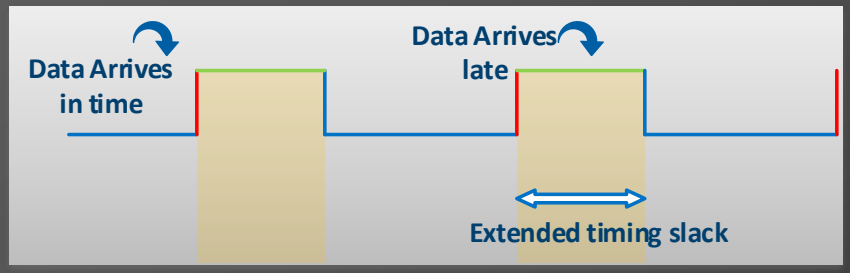


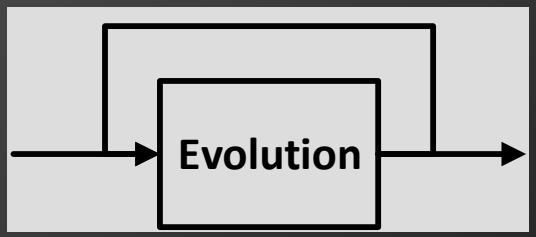
Main Latch: store correction data

Shadow FF: store data @ clk rising

Comparator: check if timing violated

CS MUX: select normal / skip

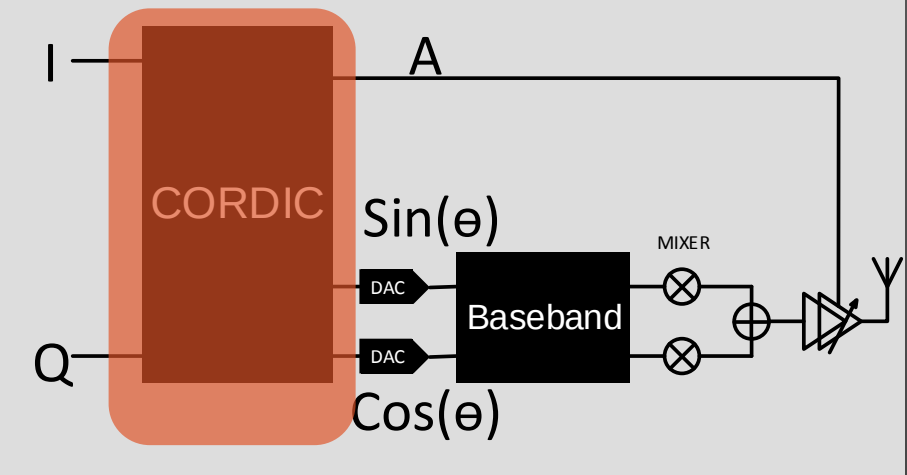




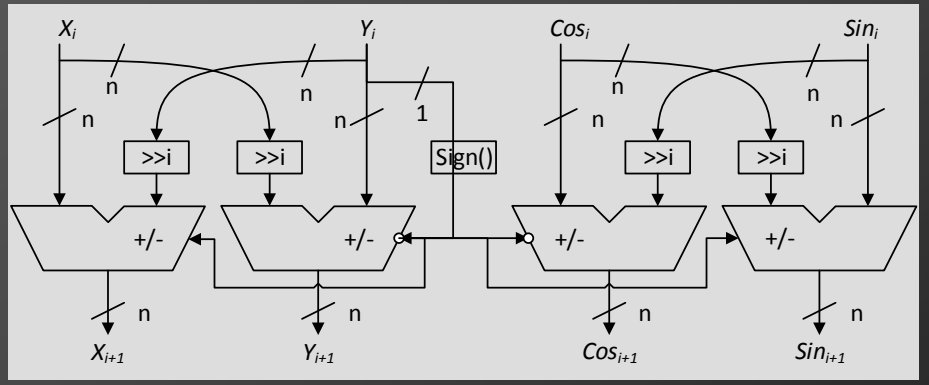
Skip the part of the logic-computation once a timing-error is detected

Skipping serves as the approximation for the logic-computation

CORDIC APPLICATION



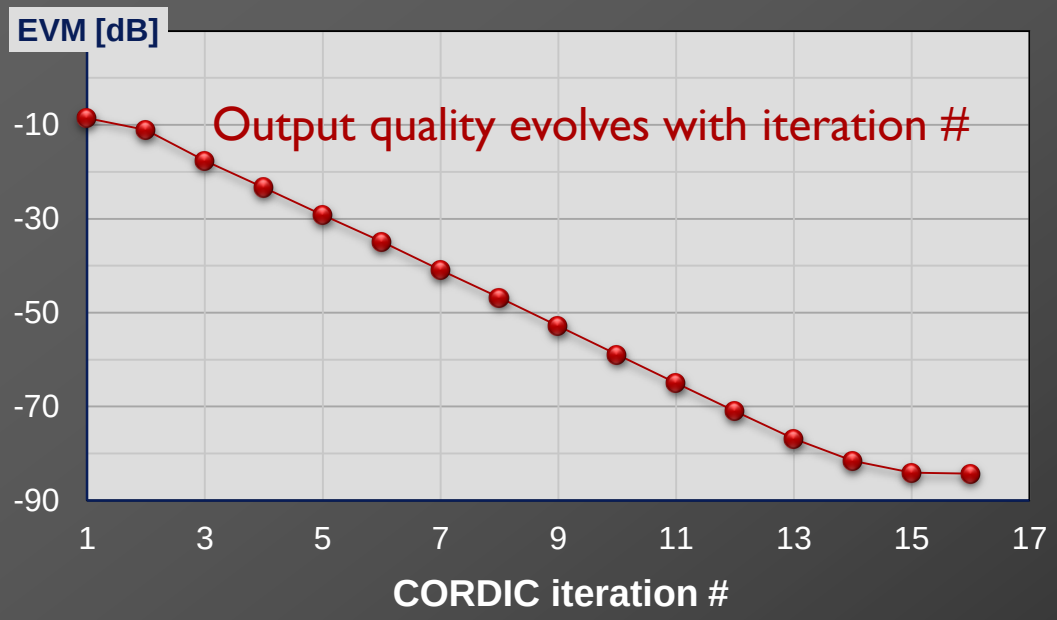
IQ to Polar conversion for polar transmitter

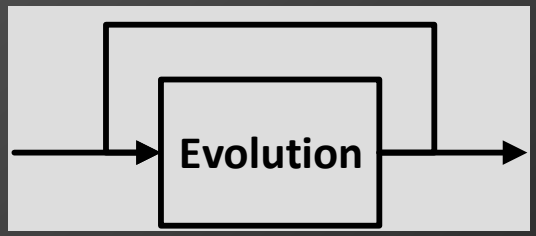


CORDIC cell

A CORDIC operation consists of several (logic) CORDIC cells

CORDIC PROPERTY

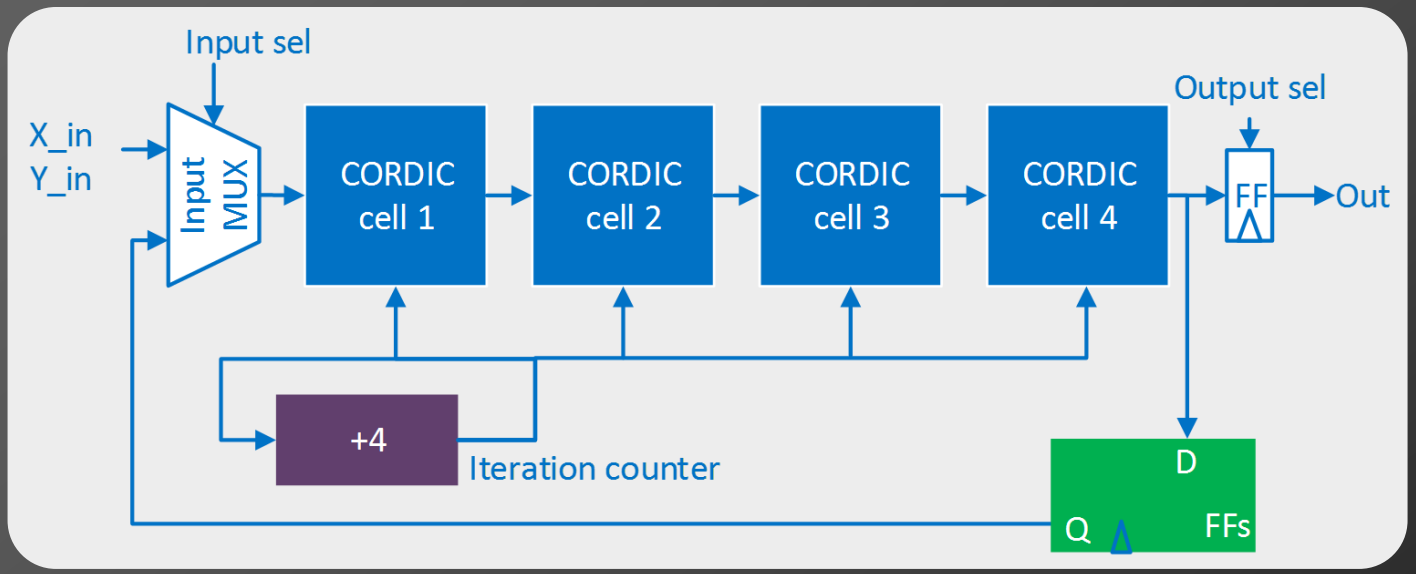




Quality (EVM) is degraded if iteration # reduces

Skipping reduces EVM, but might be accepted by later stages, e.g. analog RF

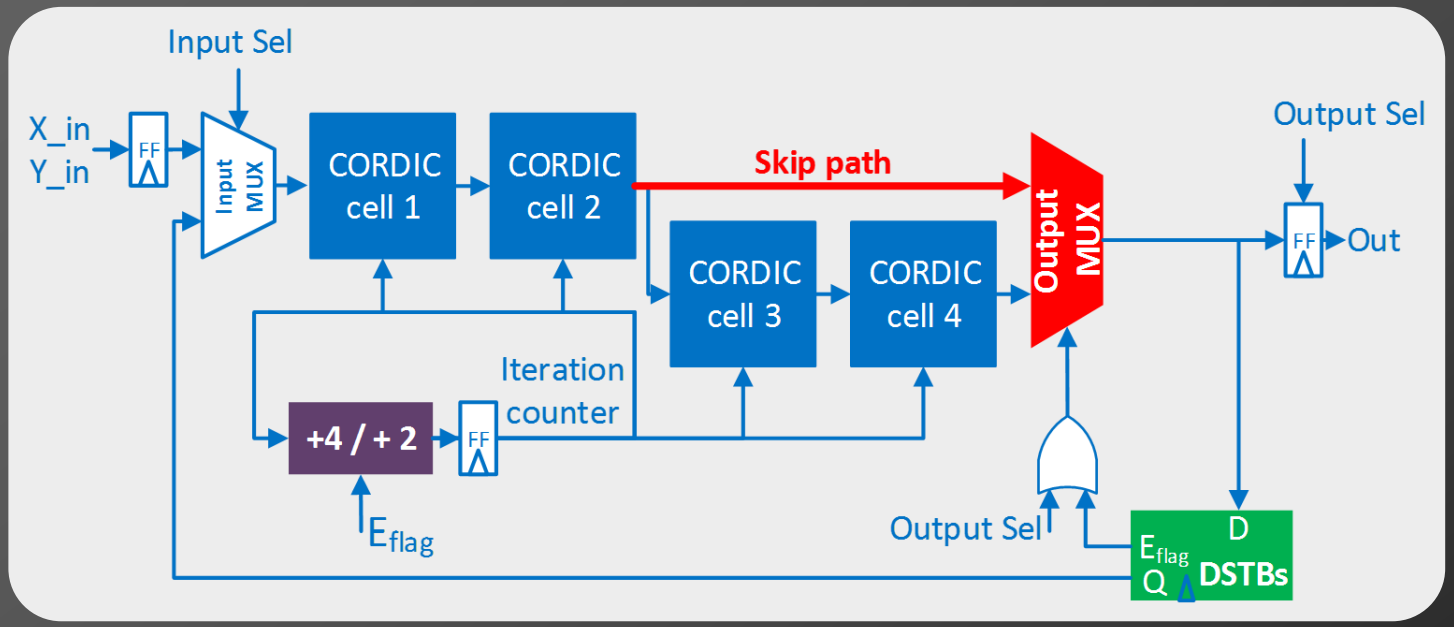
Conventional CORDIC



Conventional CORDIC

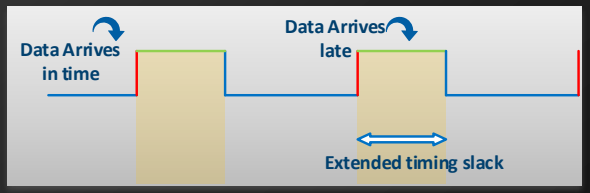
- 1 CORDIC operation = 16 iterations
- 4 cells (iterations) per cycle, 4 cycles per operation

Proposed partial CS scheme CORDIC



Partial CS CORDIC

- If timing violation from the previous cycle, skip cell 3 and cell 4
- Always skip 2 cells (2 cycles) in the last cycle
- Timing detection window = ¼ clock period



Relaxed setup timing-constraint for data-path because error will be handled

Problem Statement

Partial CS (Computation-Skip) Scheme, CORDIC

- Evaluation

  TSMC28nm

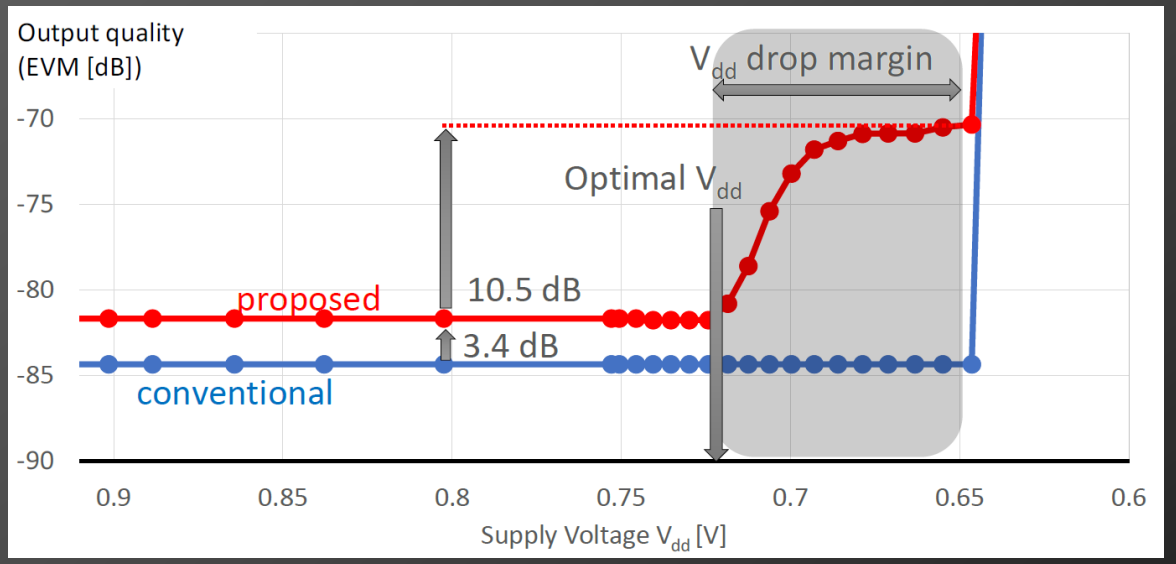
  Gate-level simulation on voltage-scaling during P&R

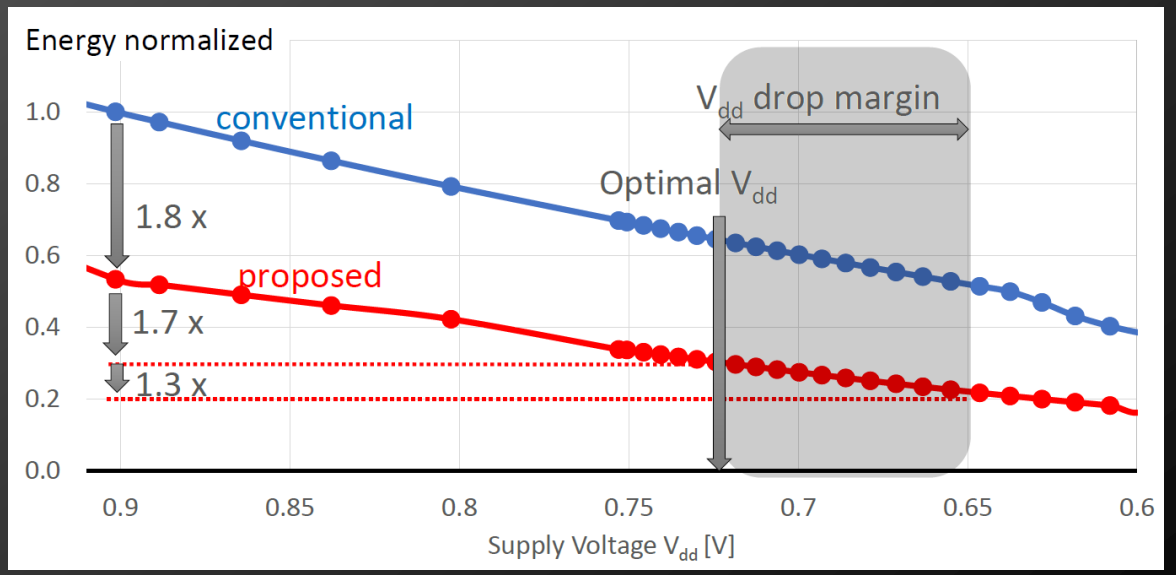
Conclusion

FIXED-FREQUENCY VOLTAGE SCALING

TSMC28nm typical case

- ❖Conv.
  - ➢ Rigid error wall
- ❖Proposed partial-CS
  - ➢ 3.4 dB worse EVM
  - ➢ Smooth error increase
  - ➢ Up to 10.5 dB worse EVM
  - ➢ 1.8X energy gain for relaxed timing constraint
  - ➢ 1.7X energy gain for error-free voltage-scaling
  - ➢ 1.3X energy gain if EVM can be degraded





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Evaluation

➢Conclusion

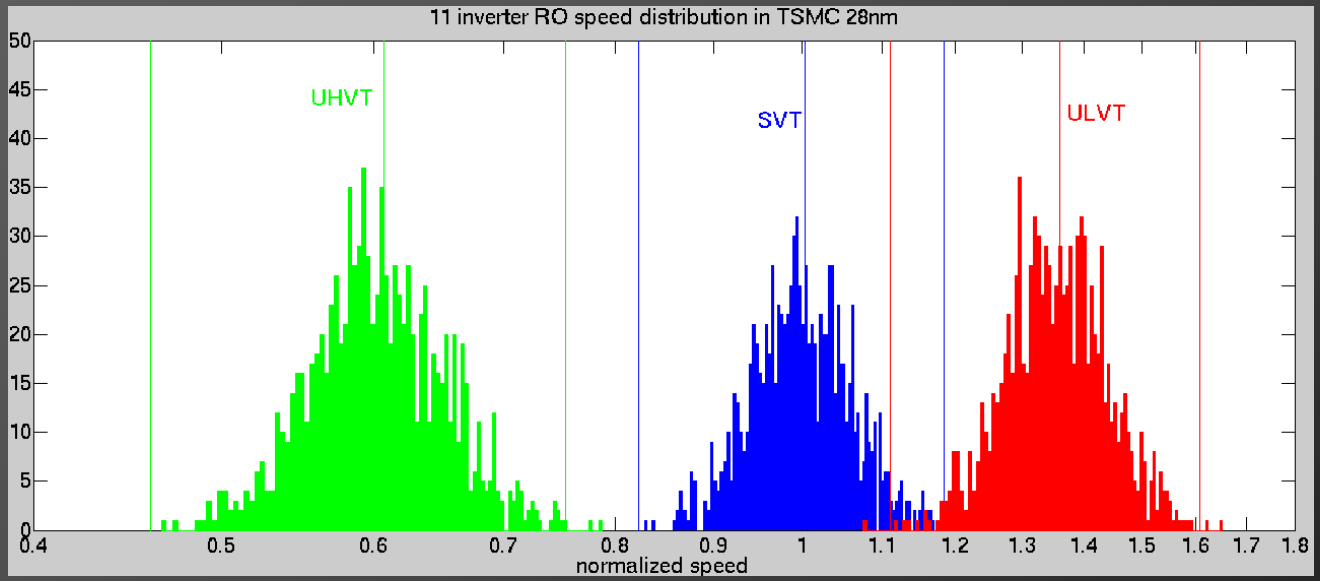
CONTRIBUTION OF THIS PAPER

- Partial CS (Computation-skip) scheme is proposed to exploit design margin
- For timing-error correction, the proposed scheme leads to quality penalty (at most 13.9 dB), but no throughput penalty
- Demonstrated on (but not limited to) recursive CORDIC.
- 1.8*1.7*1.3X (4.0X) power saving w.r.t. naïve conventional design

Thank you!

Questions?

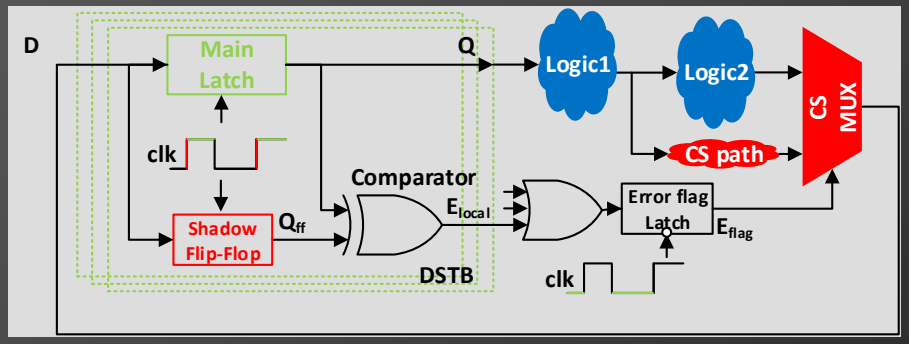
Back ups

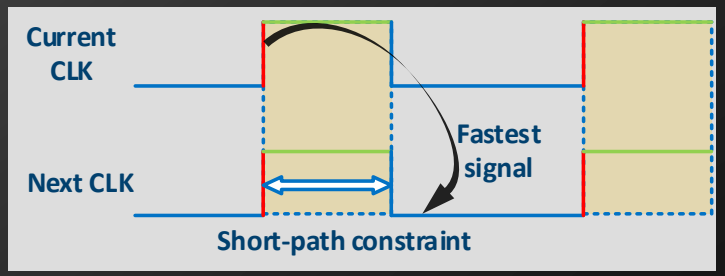

11 inverter RO speed distribution in TSMC 28nm
UHVT
SVT
ULVT
50
45
40
35
30
25
20
15
10
5
0
0.4
0.5
0.6
0.7
0.8
0.9
1
1.1
1.2
1.3
1.4
1.5
1.6
1.7
1.8
normalized speed

SHORT-PATH CONSTRAINT

Q cannot propagate to Latch too quick
Otherwise a false timing error is Triggered

- ✓ Add delay buffers automatically to fix this hold violation
- ✓ 8% power overhead





CONTROL-PATH META-STABILITY

Q_ff suffers from meta-stability, hence affects the E_local (control path)

✓Choose high gain FF, <15ps time constant for the technology.
✓Set 600ps resolution window, by far enough for MTBF