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Exploring Different Approximate Adder Architecture Implementations in a 250 °C SOI Technology

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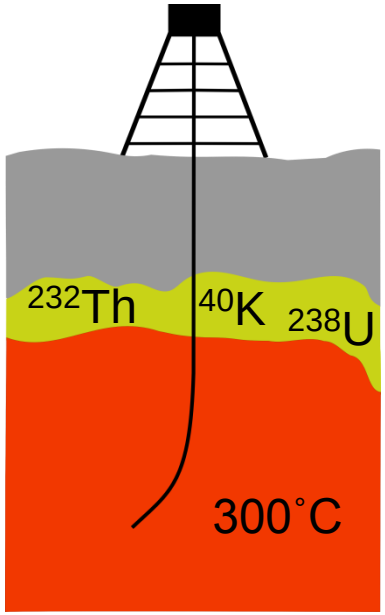
Motivation

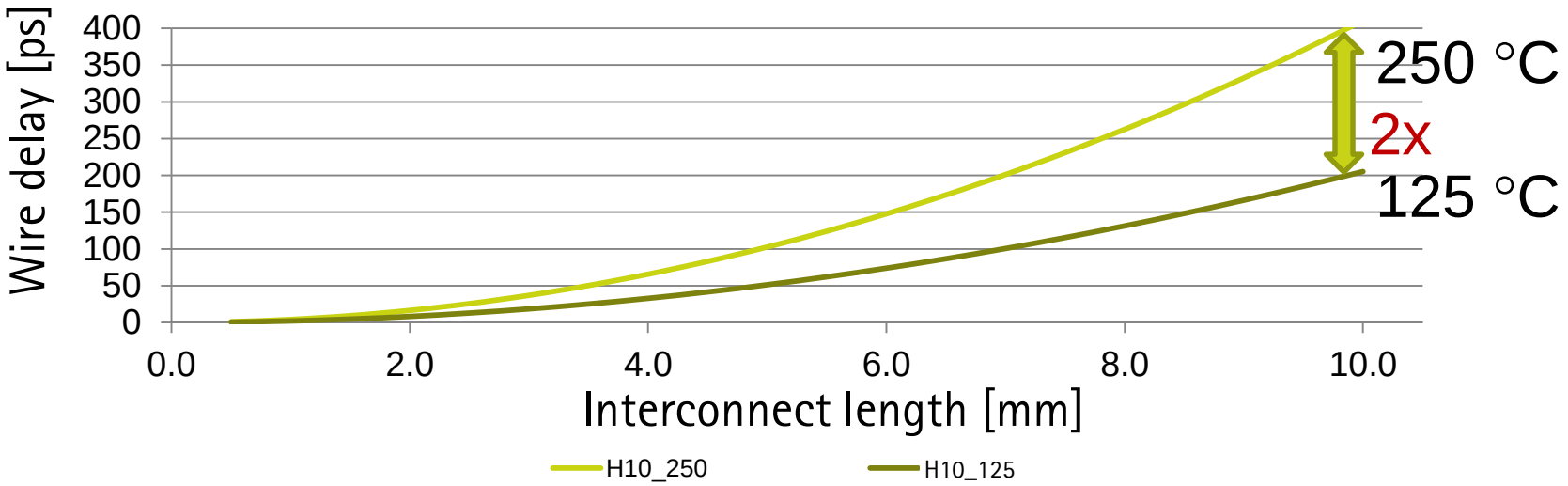
- Geothermal energy
  - Temperature range between 150 °C and 300 °C
- Drilling technology
  - Extremely limited communication bandwidth
  - → Autonomous measurement while drilling

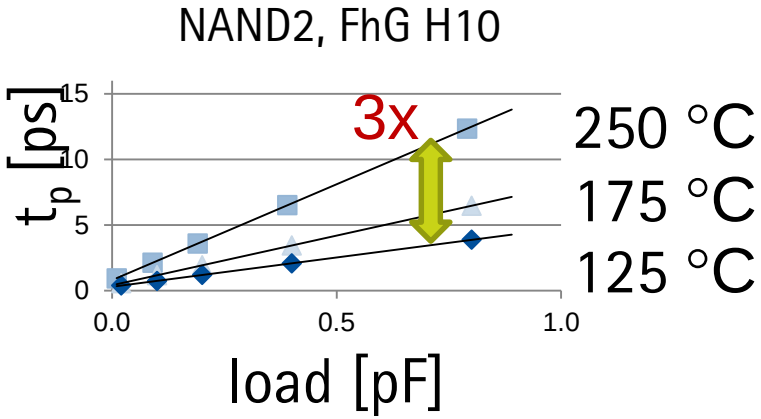
→ Microcontroller for downhole computations at 300 °C needed



- Benefits from using SOI technology:
  - Reduced leakage due to significantly smaller diode area
  - Reduced parasitic capacities due to burried oxide
  - Latch-up not possible

Temperature Dependent Delays





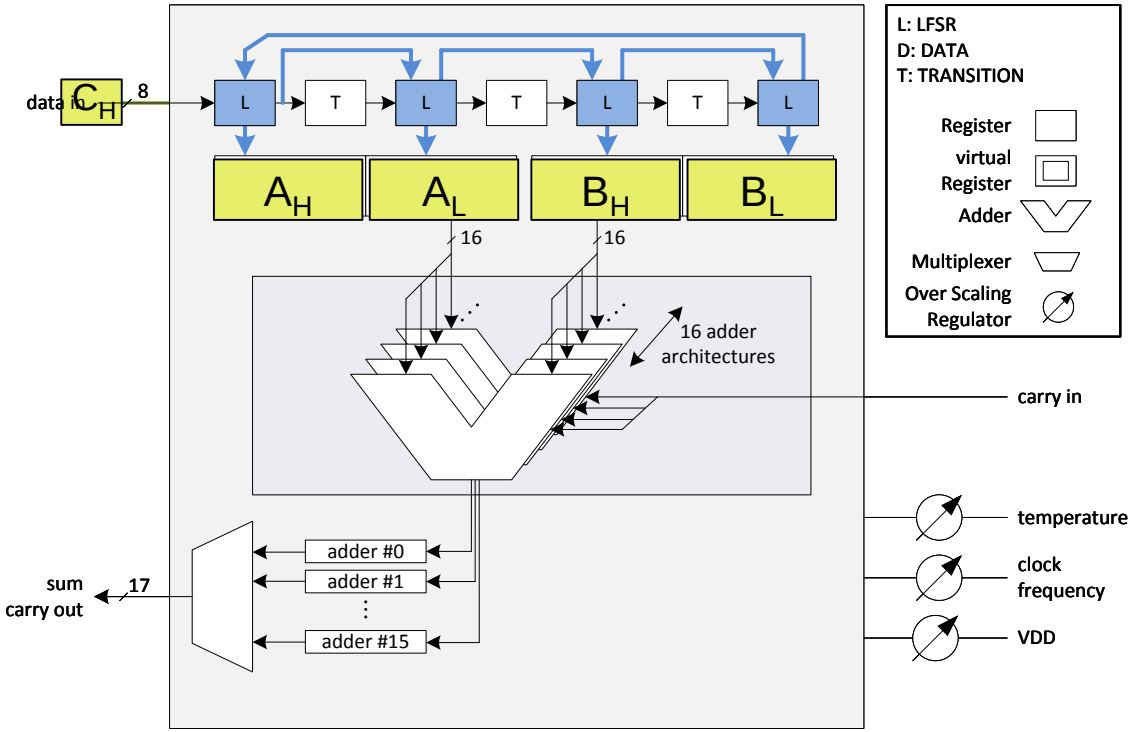
- Typically: worst case design
  - Reduced performance at very low clock
- Our approach: why not designing for lower temperatures?
  - Using approximate arithmetic architectures
  - Considering stochastic effects

→ Temperature Overscaling

Digital Architecture Design for Evaluation ASIC

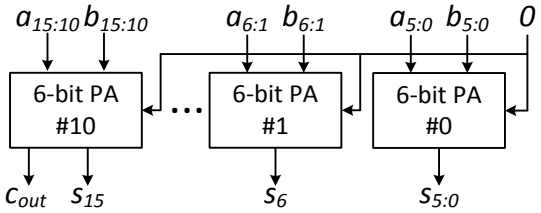
- Designed for fabrication
- Evaluation of 16 adders (16-bit operands)
  - Critical path lies within adders
- Perform overscaling
  - Frequency
  - Voltage
  - Temperature
- Two operation modes
  - External data
  - LFSR

1. A+B
2. C+D



Architecture Design
Implemented Adders

- Precise Adder (PA)
  - Ripple-Carry-Adder
  - Carry-Lookahead-Adder
  - Carry-Select-Adder
- Almost-Correct-Adder (ACA) [1]
  - Limited maximal length of carry propagation
  - Example: 16-bit ACA-RCA4



Max. carry-propagation	ACA accuracy
4	80.35%
6	95.71%
8	99.12%
10	99.83%
12	99.97%

  - Limited theoretical accuracy by design
  - ACA-RCA4, ACA-RCA6, ACA-RCA8, ACA-RCA10, ACA-RCA12

[1] Verma, Brisk, Ienne, „Variable latency speculative addition: A new paradigm for arithmetic circuit design", 2008

Architecture Design
Implemented Adders

- Precise Adder (PA)
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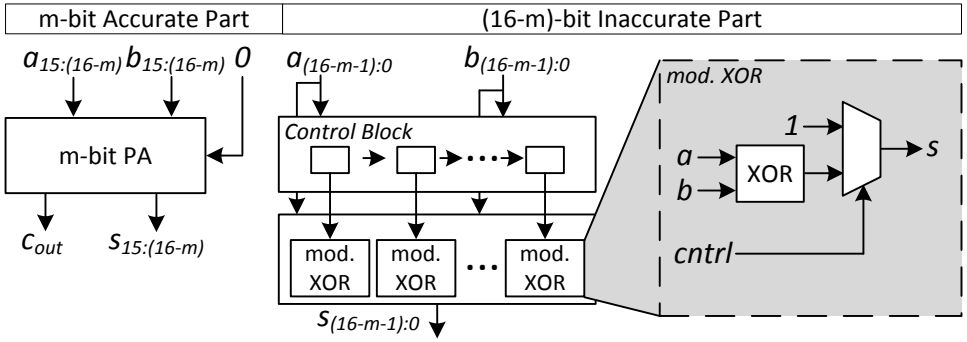
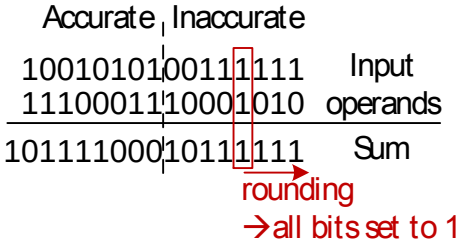
  - Carry-Lookahead-Adder
  - Carry-Select-Adder
- Almost-Correct-Adder (ACA) [1]
- Error-Tolerant-Adder (ETA) [2]
  - Inaccurate part rounds result up





  - ETA-FIX-4, ETA-FIX-6, ETA-FIX-8, ETA-FIX-10, ETA-FIX-12

[1] Verma, Brisk, Ienne, „Variable latency speculative addition: A new paradigm for arithmetic circuit design", 2008
[2] Zhu, Goh, Zhang, Yeo, Kong, „Design of low-power high-speed truncation-error-tolerant adder and its application in digital signal processing", 2010

Evaluation Methodology

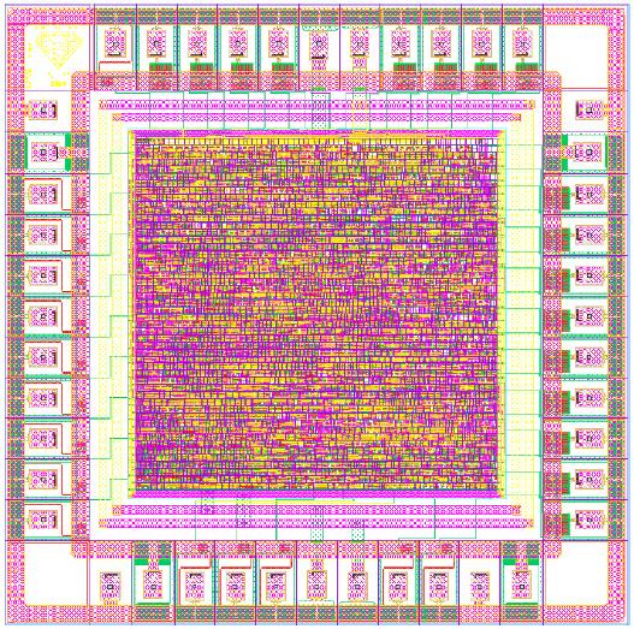
- Chip design using Fraunhofer-H10 SOI technology (1µm)
  - Extract parasitics (gate delays and wire delays) into SDF file
- Modelsim gate-level simulation of chip design
  - Using SDF file from chip layout
  - Considering delays in simulation
- 50,000 random operations
- Overclocking up to a K-factor of 6

$$K = \frac{T_{critical}}{T_{overscale}} = \frac{f_{overscale}}{f_{max}}$$

- Error metric (position where error occurs):

$$\epsilon = \mathrm{ld}\lfloor |sum - reference| \rfloor$$

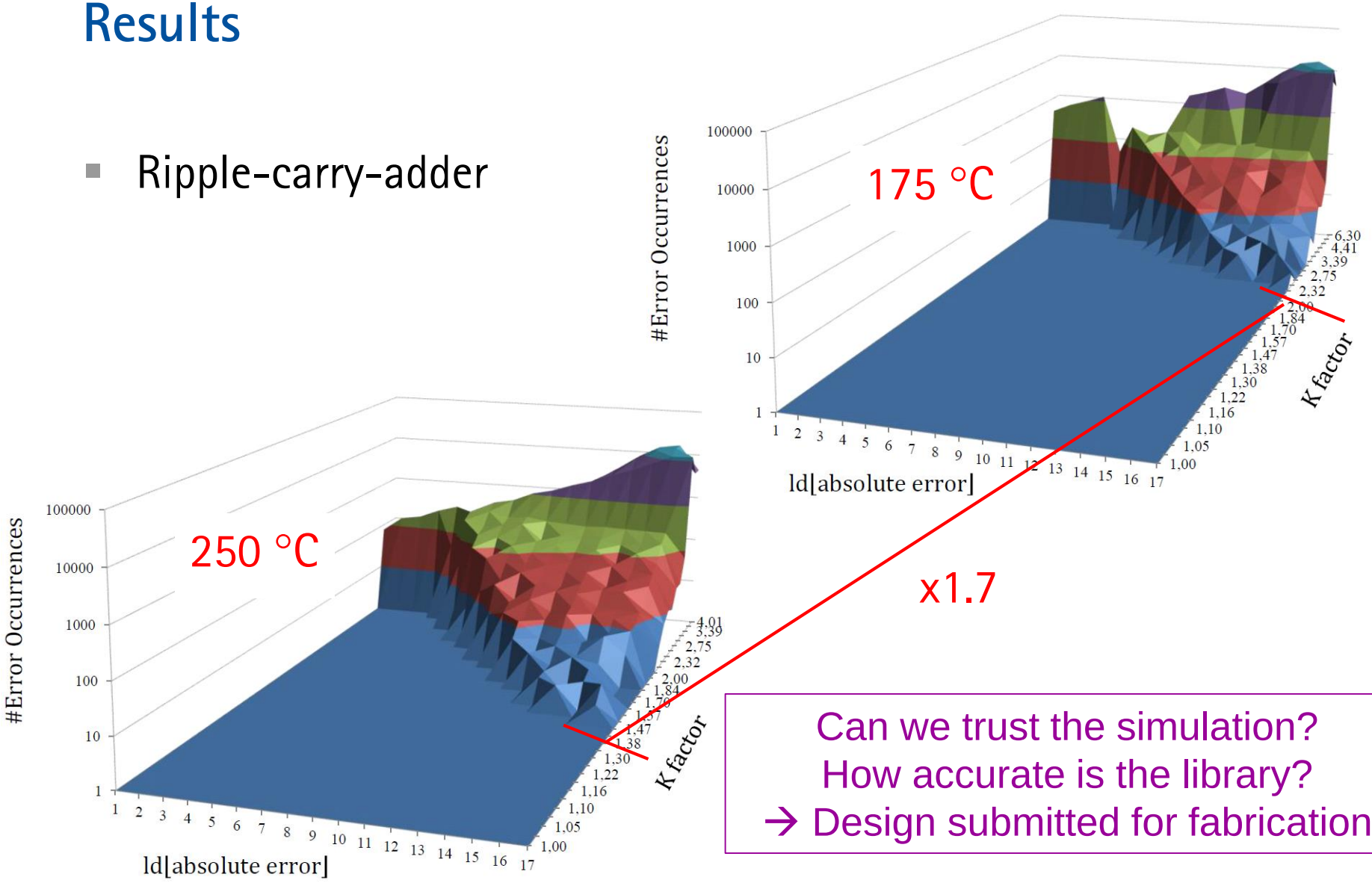
- Using two corner cases from library
  - 175 °C@3,3V (typ.)
  - 250 °C@3,3V (WC)



- 3.37 mm x 3.35 mm

Results

- Ripple-carry-adder

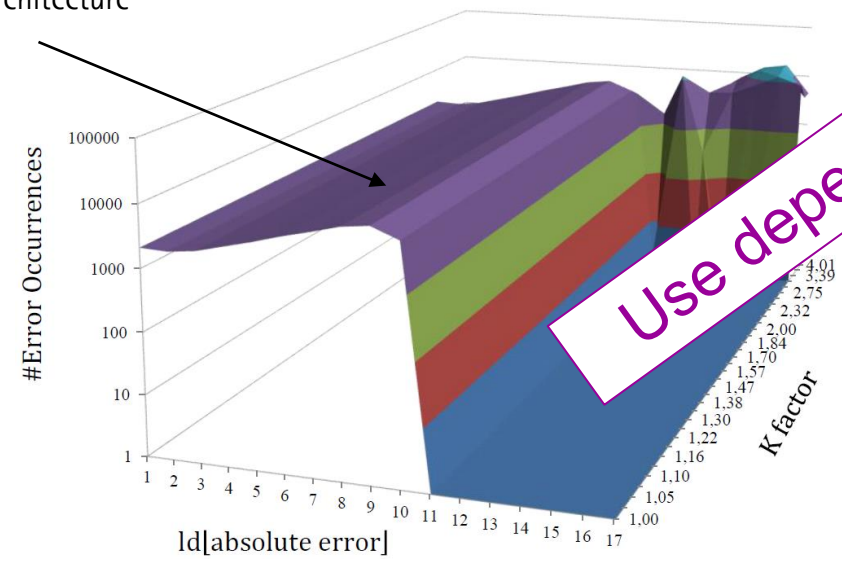


Can we trust the simulation?
How accurate is the library?
→ Design submitted for fabrication

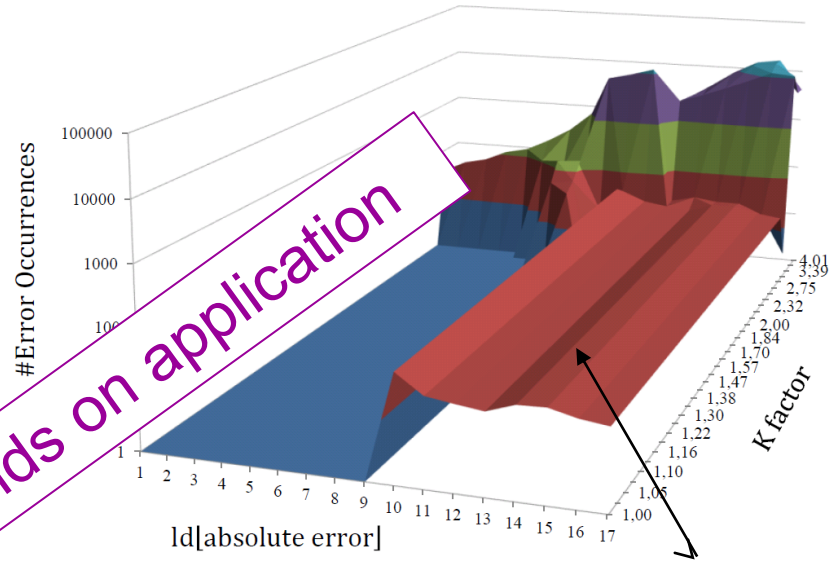
Results

- Simulation at 250 °C

Approximation error due to architecture



Use depends on application



Approximation error due to architecture

ETA-FIX-6

Accuracy: 3%

Error characteristic: **frequent small** magnitude errors

Area requirements: 42,000 µm²

ACA-RCA8

Accuracy: 99.5%

Error characteristic: **infrequent large** magnitude errors

Area requirements: 155,000 µm²

Area requirements RCA: 66,000 µm²

Summary / Future Work

- Different adder architectures have been evaluated for their characteristics in high temperature VLSI implementation
  - Frequency overscaling at temperatures 175 °C and 250 °C
- Path delay increases by a factor of **1.7x** from 175 °C to 250 °C
- Results can be used to develop high temperature applications which can operate **beyond** the specified maximum temperature range

- Future Work
  - Consider more complex arithmetic elements that include adders in their critical path (e.g., multipliers, CORDIC)
  - Repeat experiments on real chip after fabrication (frequency, voltage, temperature overscaling)